3D integrated physics package using hybrid assembly process for chip-scale atomic clocks

Yeeun Na[1], Chaehwan Kim[1], Il-Suk Kang[1], Yeon-Wha Oh[1], Jong-Bum You[1], Boo Taek Lim[1], Soo-Hyun Kwon[1], Eui-Je Jo[1], Jong Hyun Song[1], Seung-In Lee[1], Byung Il Lee[1], Hyun-Gue Hong[2], Sang Eon Park[2], Taeg Yong Kwon[2], Tae-Hyun Jun[3], Hyun Jin Choi[3], Jongcheol Park[1]

[1]Center for Next-Generation Platform Development, National Nano Fab Center, Daejeon, Korea
[2]Time and Frequency Group, Korea Research Institute of Standards and Science, Daejeon, Korea
[3]Datalink Group, DUKSAN Navcours Co.,Ltd., Daejeon, Korea

Email: jcpark@nnfc.re.kr

The evolution of timing references has encouraged advancements in miniaturization and low power consumption, exemplified by the development of chip-scale atomic clocks (CSACs) for aerospace, radio communication, and GPS [1, 2]. The first prototype of a commercial CSAC product achieved a volume of 10 cm³ following S. Knappe et al.'s introduction of the chip-scale physics package. Although the CSAC has been commercialized more than decade, its widespread is limited because the fabrication technology of the physics package is not sufficiently matured. In this paper, we present the 3D integration of physics package using hybrid assembly process, aiming for miniaturization and low power consumption while increasing the accessibility of CSAC fabrication. The proposed assembly process consists of the matured planar process and 3D assembly as shown in Fig. 1 (a). For miniaturization, the octagonal-shaped Si PD with inradius of 1.5 mm was fabricated by using the plasma dicing process and the cross shaped Cs vapor cell was manufactured through a micromachining process. The VCSEL was utilized for optical transition of Cs in the MEMS vapor cell. The linear-polarized beam from the VCSEL is converted using an in-house QWP with a ND filter by using single crystal quartz with a metallic thin film. The planar process was conducted on a flexible printed circuit (FPC) with a planar coil pair by integrating the VCSEL, thermistor, PD, and a pair of thin-film heaters with a resistance of 60Ω, as depicted in Fig. 1 (a). Subsequently, the aligning parts using aluminum machining was assembled on the FPC for precise alignment and thermal management of the physics package. The 3D integration was implemented by folding and stacking the FPC using the mu-metal supports to suspend the FPC for enhanced thermal resistance and serve as a magnetic shield for the physics package. The prototype of physics package has volume of 7×7×7 mm³. Fig. 1 (b) and (c) show the photography and experimental results of physics package. The proposed physics package has the CPT line width of 7.4 kHz with an operational power consumption of about 224 mW. The experimental results of the proposed physics package presented promising advancements in CSACs by facilitating accessibility of fabrication, demonstrating its potential for widespread application in various fields.

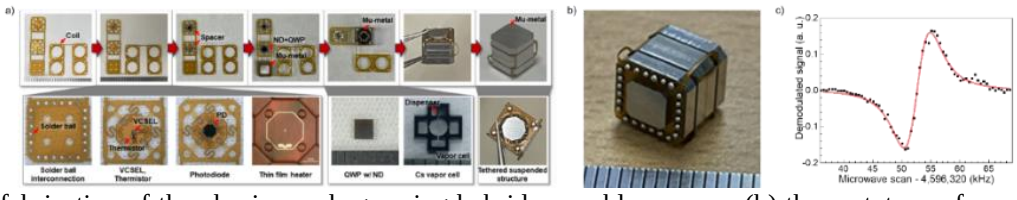

Fig. 1: (a) fabrication of the physics package using hybrid assembly process, (b) the prototype of proposed physics package, and (c) CPT resonance of physics package.

[1] S. Knappe et al., "A microfabricated atomic clock", Appl. Phys. Lett., vol. 85, pp. 1460-1462, 2004.

[2] R. Lutwak et al., "The Chip-Scale Atomic Clock-Prototype Evaluation", 39th PTTI Meeting, pp. 269-290, 2007.